The following claims are presented for examination:

Claim 1. (withdrawn) An apparatus comprising:

a first transistor having a gate, a source, and a drain;

a second transistor having a gate, a source, and a drain, wherein the gate of said second transistor is electrically connected to the gate of said first transistor, and wherein the source of said first transistor is electrically connected to the source of said second transistor;

a first resistor having a first terminal and a second terminal, wherein the first terminal of said first resistor is electrically connected to the drain of said first transistor;

a first capacitor having a first terminal and a second terminal, wherein the first terminal of said first capacitor is electrically connected to the drain of said first transistor;

a second resistor having a first terminal and a second terminal, wherein the first terminal of said second resistor is electrically connected to the drain of said second transistor; and

a second capacitor having a first terminal and a second terminal, wherein the first terminal of said second capacitor is electrically connected to the drain of said second transistor.

Claim 2. (withdrawn) The apparatus of claim 1 wherein the second terminal of said first capacitor is electrically connected to ground, and wherein the second terminal of said second capacitor is connected to ground.

Claim 3. (withdrawn) The apparatus of claim 1 wherein the source of said first transistor is electrically connected to a positive voltage.

Claim 4. (withdrawn) An apparatus comprising:

a first transistor having a gate, source, and a drain, wherein said gate of said first transistor is electrically connected to said drain of said first transistor;

a second transistor having a gate, source, and a drain, wherein said gate of said second transistor is electrically connected to said drain of said second transistor, and wherein said source of said second transistor is electrically connected to drain of said first transistor;

a third transistor having a drain, gate, and source, wherein said gate of said third transistor is electrically connected to said drain of said third transistor, and wherein said source of said third transistor is electrically connected to said drain of said second transistor; and

a capacitor having a first terminal and a second terminal, wherein said first terminal of said capacitor is electrically connected to said drain of said second transistor.

Claim 5. (withdrawn) The apparatus of claim 4 wherein said first transistor is a PMOS transistor, wherein said second transistor is a PMOS transistor, and wherein said third transistor is a PMOS transistor.

Claim 6. (withdrawn) The apparatus of claim 4 wherein the first terminal of said capacitor is electrically connected to a bias input terminal of a bandgap reference voltage generator.

Claim7 (currently amended) An apparatus comprising:

a bandgap reference voltage generator having an output terminal;

an operational amplifier having a positive input terminal, a negative input terminal, and an output terminal, wherein the positive input terminal of said operational amplifier is electrically connected to the output terminal of said bandgap reference voltage generator;

a transistor having a gate, a source, and a drain, wherein the gate of said transistor is electrically connected to the output of said operational amplifier, and wherein the drain of said transistor is electrically connected to the negative input terminal of said operational amplifier; ~~and~~

a voltage divider having a input terminal, an output terminal, and a common terminal, wherein said input terminal of said voltage divider is electrically connected to the negative input terminal of said operational amplifier**;**

a startup network having a positive supply terminal and an output terminal, wherein said output terminal of said startup network is electrically connected to said input terminal of said voltage divider; and

a self-biasing network having a positive supply terminal, a common terminal, and an output terminal, wherein said positive supply terminal of said self-biasing network is electrically connected to said output terminal of said startup network, and wherein said common terminal of said self-biasing network is electrically connected to said common terminal of said voltage divider.

Claim 8. (original) The apparatus of claim 7 wherein said transistor is a PMOS transistor.

Claims 9 and 10. (canceled)

Claim 11. (currently amended) The apparatus of claim ~~10~~ **7** wherein said bandgap voltage reference generator also comprises a bias terminal, and wherein said output terminal of said self-biasing network is electrically connected to the bias terminal of said bandgap voltage reference generator.

Claim 12. (currently amended) The apparatus of claim ~~10~~ 7 wherein said operational amplifier also comprises a bias terminal, and wherein said output terminal of said self-biasing network is electrically connected to said bias terminal of said operational amplifier.

Claim 13. (currently amended) The apparatus of claim ~~10~~ 7 wherein said bandgap reference voltage generator further comprises a positive supply terminal and a common terminal, and wherein said operational amplifier also comprises a positive supply terminal and a common terminal, and wherein said positive supply terminal of said bandgap reference voltage generator is electrically connected to said positive supply terminal of said operational amplifier, and said common terminal of said bandgap reference voltage generator is electrically connected to said common terminal of said operational amplifier.

Claim 14. (currently amended) The apparatus of claim 13 wherein ~~and~~ said common terminal of said voltage divider is electrically connected to said common terminal of said operational amplifier.

Claim 15. (original) The apparatus of claim 13 wherein said positive supply terminal of said startup network is electrically connected to said positive supply terminal of said operational amplifier.

Claim 16. (original) The apparatus of claim 13 wherein said source terminal of said transistor is electrically connected to said positive supply terminal of said operational amplifier.

Claim 17. (original) The apparatus of claim 14 wherein said bandgap reference voltage generator further comprises a first capacitor having a first terminal and a second terminal, wherein:

said first terminal of said first capacitor is electrically connected to said output terminal of said bandgap reference voltage generator; and

said second terminal of said first capacitor is electrically connected to said common terminal of said bandgap reference voltage generator.

Claim 18. (original) The apparatus of claim 17 wherein said operational amplifier further comprises a second capacitor having a first terminal and a second terminal, wherein:

said first terminal of said second capacitor is electrically connected to said negative input terminal of said operational amplifier; and

said second terminal of said second capacitor is electrically connected to said common terminal of said operational amplifier.

Claim 19. (original) The apparatus of claim 18 wherein said voltage divider further comprises a third capacitor having a first terminal and a second terminal, wherein:

said first terminal of said third capacitor is electrically connected to said output terminal of said voltage divider; and

said second terminal of said third capacitor is electrically connected to said common terminal of said voltage divider.

Claim 20. (original) The apparatus of claim 19 wherein said self-biasing network further comprises a fourth capacitor having a first terminal and a second terminal, wherein:

said first terminal of said fourth capacitor is electrically connected to said output terminal of said self-biasing network; and

said second terminal of said fourth capacitor is electrically connected to said common terminal of said self-biasing network.